



# STW45NM50FD

N-channel 500V - 0.07 $\Omega$  - 45A - TO247  
FDmesh™ Power MOSFET (with fast diode)

## General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STW45NM50FD	500V	<0.1 $\Omega$	45A

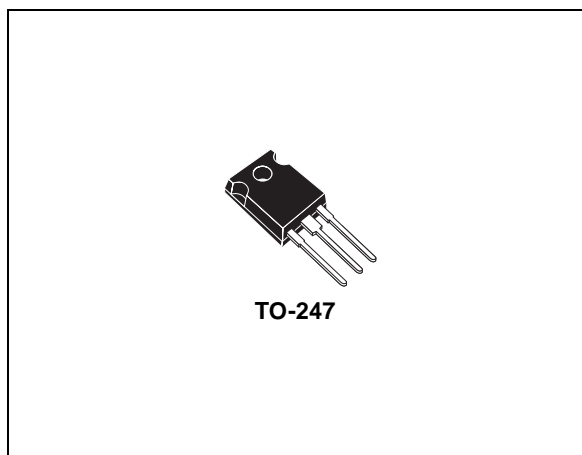
- 100% avalanche tested
- High dv/dt and avalanche capabilities
- Low input capacitance and gate charge
- Low gate input resistance
- Tight process control and high manufacturing yields

## Description

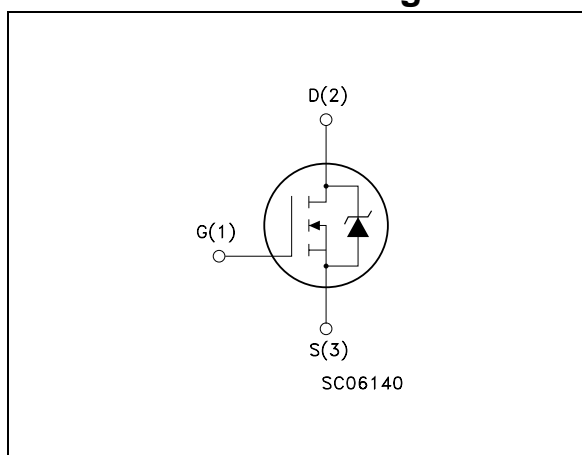
The FDmesh™ associates all advantages of reduced on-resistance and fast switching with an intrinsic fast-recovery body diode. It is therefore strongly recommended for bridge topologies, in particular ZVS phase-shift converters.

## Applications

- Switching application



## Internal schematic diagram



## Order codes

Part number	Marking	Package	Packaging
STW45NM50FD	W45NM50FD	TO-247	Tube

# Contents

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	500	V
$V_{DGR}$	Drain-gate voltage ( $R_{GS} = 20K\Omega$ )	500	V
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ C$	45	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ C$	28.4	A
$I_{DM}^{(1)}$	Drain current (pulsed)	180	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ C$	417	W
	Derating factor	2.08	W/°C
$dv/dt^{(2)}$	Peak diode recovery voltage slope	20	V/ns
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	-65 to 150	°C

1. Pulse width limited by safe operating area

2.  $I_{SD} \leq 45A$ ,  $di/dt \leq 400A/\mu s$ ,  $V_{DD} = 80\%V_{(BR)DSS}$

**Table 2. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case Max	0.3	°C/W
$R_{thj-a}$	Thermal resistance junction-ambient Max	30	°C/W
$T_l$	Maximum lead temperature for soldering purpose	300	°C

**Table 3. Avalanche data**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J$ Max)	22.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25^\circ C$ , $I_d = I_{AR}$ , $V_{DD} = 50V$ )	800	mJ

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu A, V_{GS} = 0$	500			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating @ } 125^{\circ}C$			10 100	$\mu A$ $\mu A$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 30V$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 22.5A$		0.07	0.10	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 22.5A$		20		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25V, f = 1 \text{ MHz},$ $V_{GS} = 0$		3600 1260 80		pF pF pF
$C_{oss eq.}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0V \text{ to } 400V$		350		pF
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 400V, I_D = 45A$ $V_{GS} = 10V$ (see Figure 13)		92 22 40	120	nC nC nC
$R_G$	Gate input resistance	$f = 1 \text{ MHz}$ Gate DC Bias = 0 test signal level = 20mV open drain		2		$\Omega$

1. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%
2.  $C_{oss eq.}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time Rise time	$V_{DD}=250\text{ V}$ , $I_D=22.5\text{ A}$ , $R_G=4.7\Omega$ , $V_{GS}=10\text{ V}$ (see Figure 14)		28 28		ns ns
$t_{r(Voff)}$ $t_f$ $t_c$	Off-voltage rise time Fall time Cross-over time	$V_{DD}=400\text{ V}$ , $I_D=45\text{ A}$ , $R_G=4.7\Omega$ , $V_{GS}=10\text{ V}$ (see Figure 14)		11 25 44		ns ns ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				45	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				180	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=45\text{ A}$ , $V_{GS}=0$			1.5	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=45\text{ A}$ , $T_j=25^\circ\text{C}$ $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD}=100\text{ V}$ , (see Figure 17)		200 1600 16		ns nC A
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=45\text{ A}$ , $T_j=150^\circ\text{C}$ $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD}=100\text{ V}$ , (see Figure 17)		324 4017 24.8		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

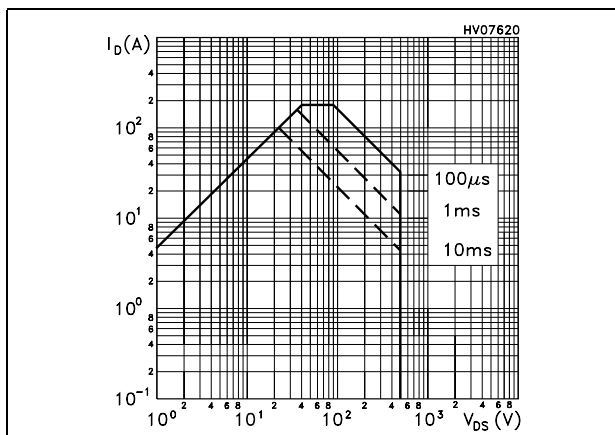


Figure 2. Thermal impedance

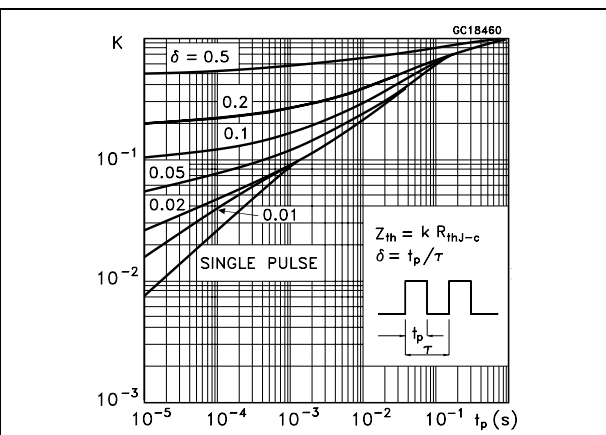


Figure 3. Output characteristics

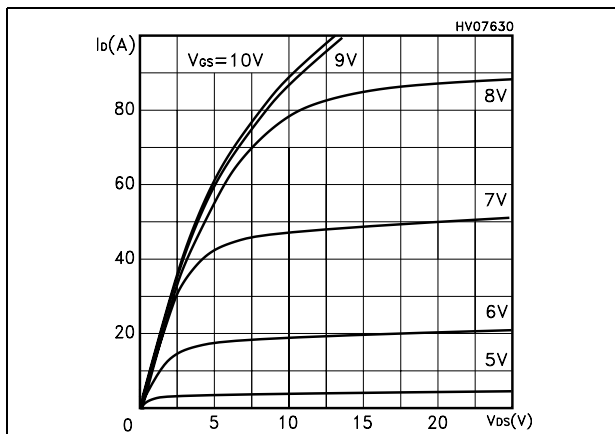


Figure 4. Transfer characteristics

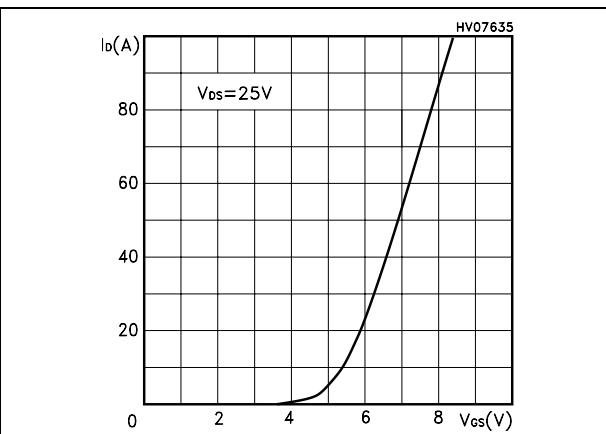


Figure 5. Transconductance

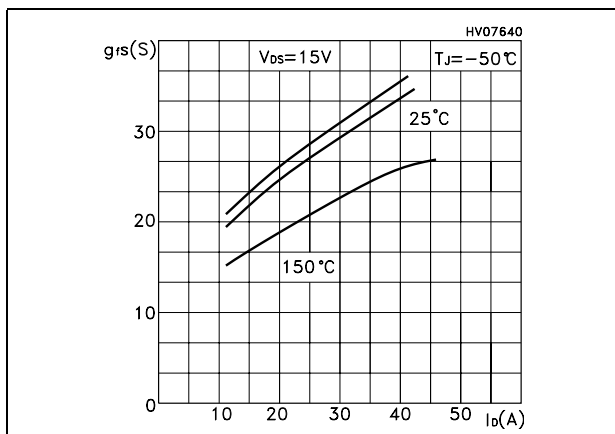


Figure 6. Static drain-source on resistance

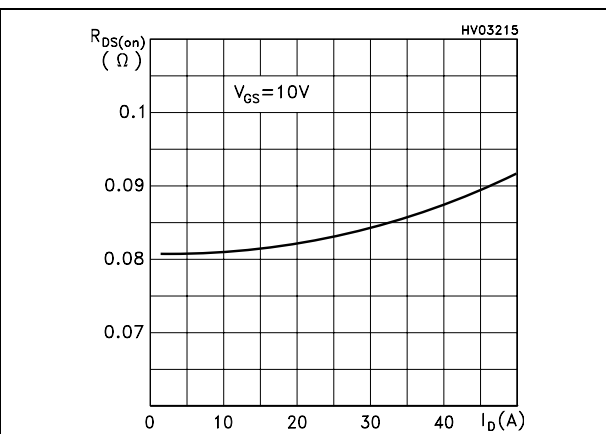


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

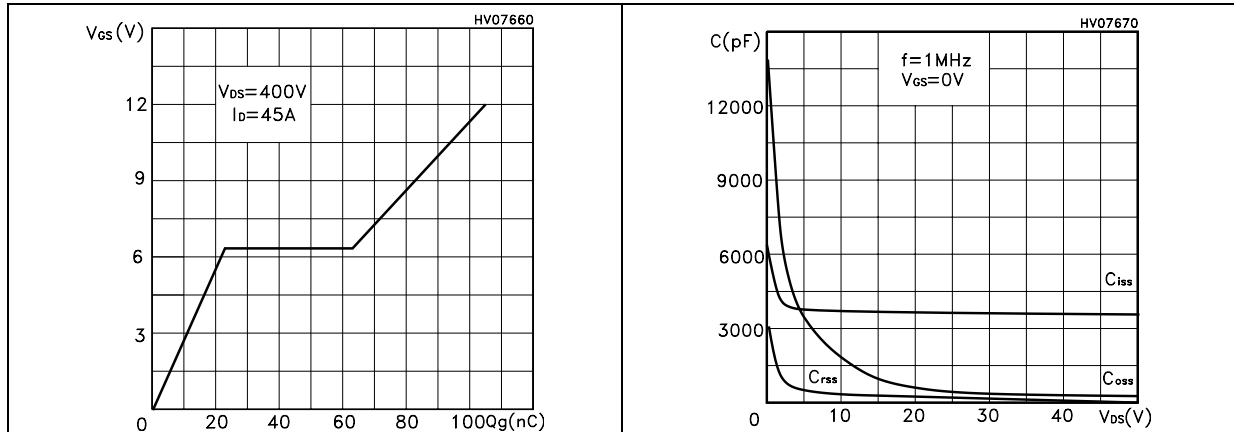


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

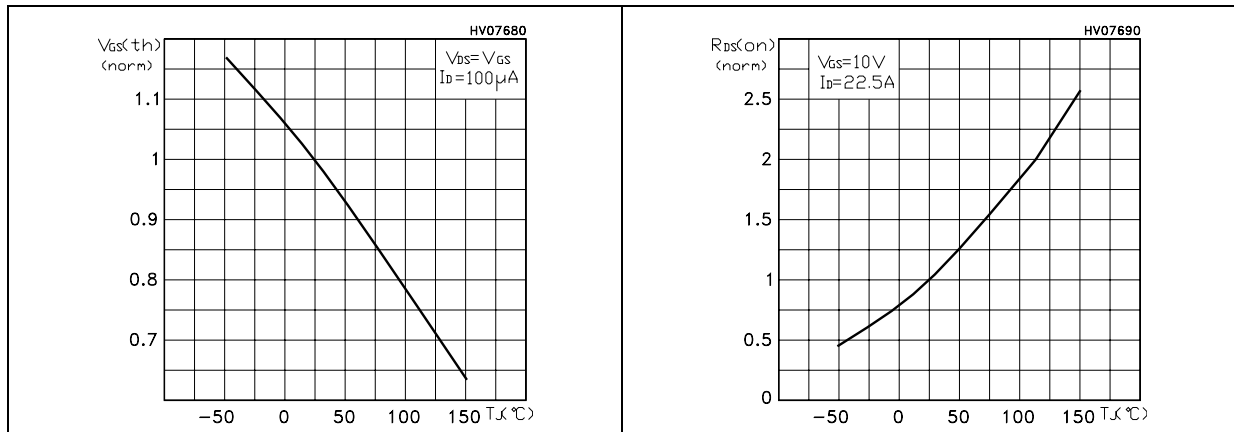
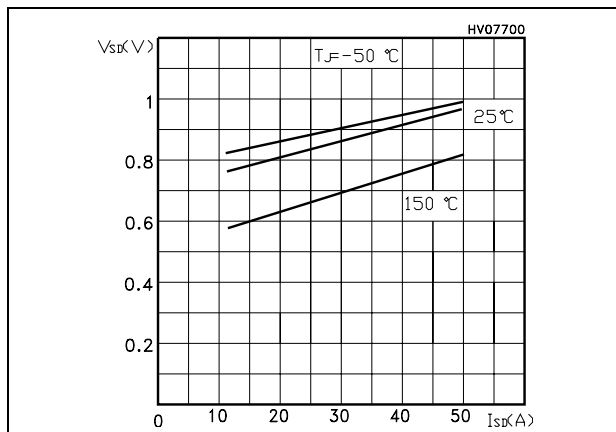


Figure 11. Source-drain diode forward characteristics



### 3 Test circuit

Figure 12. Switching times test circuit for resistive load

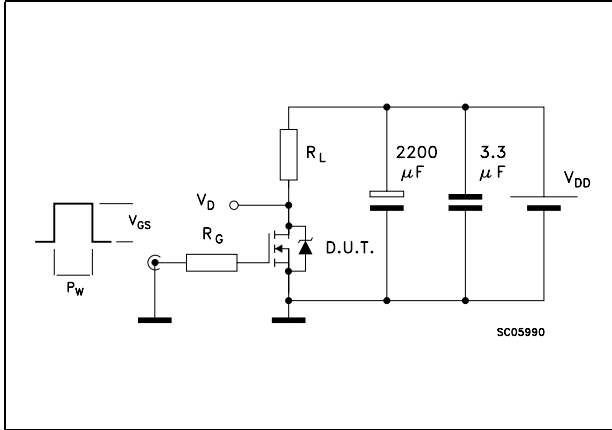


Figure 13. Gate charge test circuit

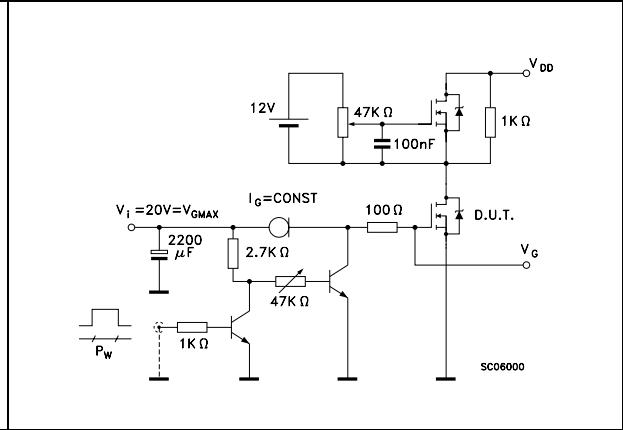


Figure 14. Test circuit for inductive load switching and diode recovery times

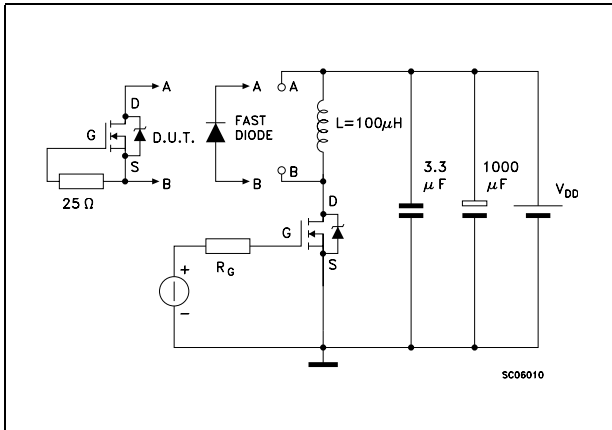


Figure 15. Unclamped inductive load test circuit

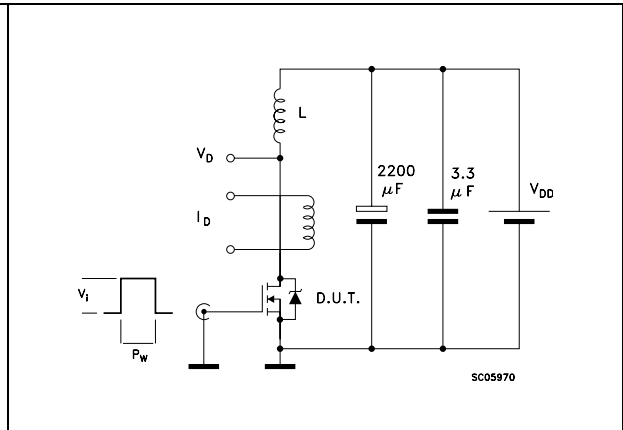


Figure 16. Unclamped inductive waveform

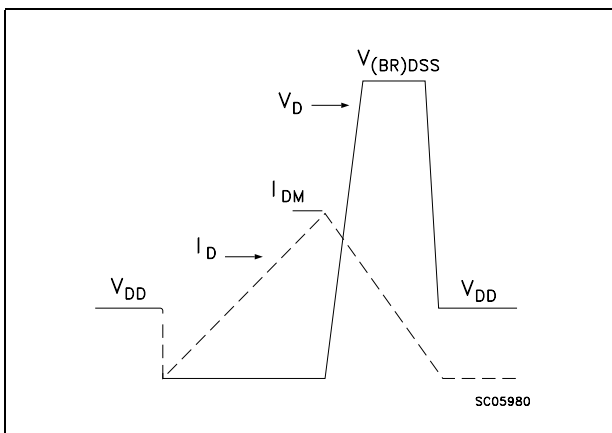
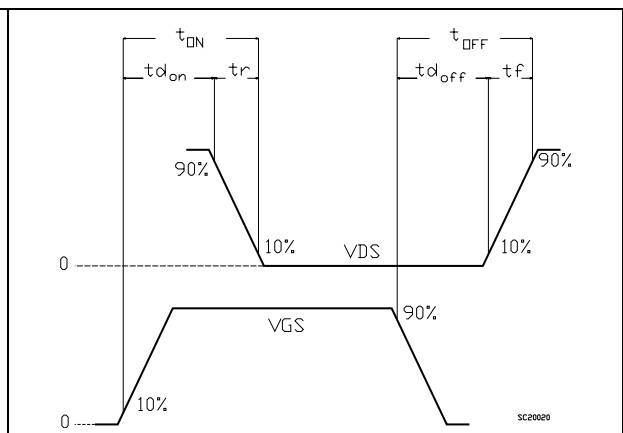


Figure 17. Switching time waveform



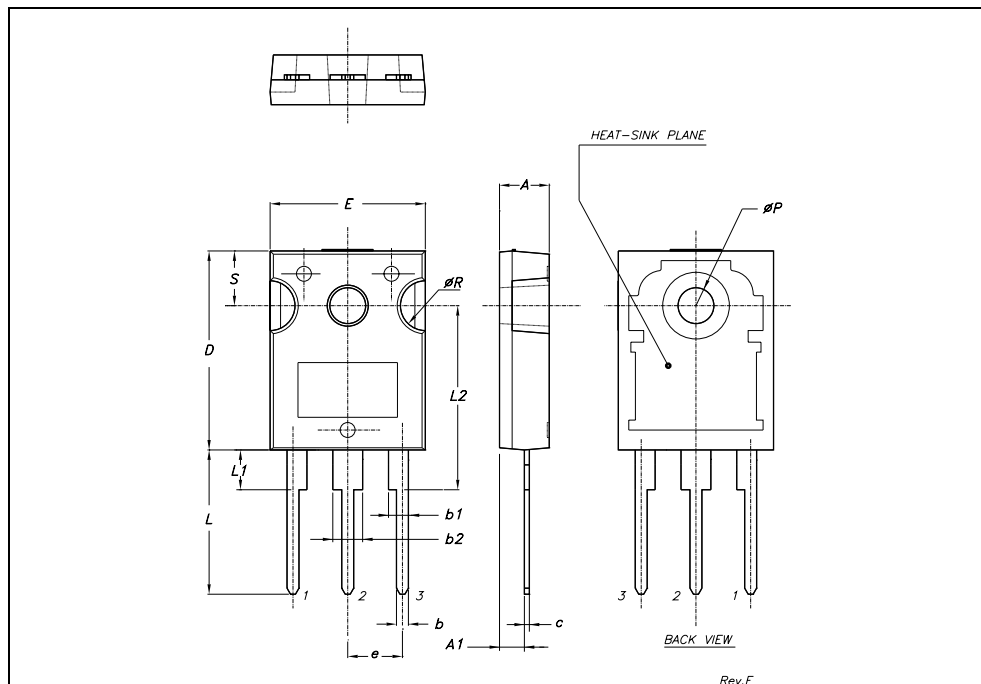


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

**TO-247 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



## 5 Revision history

**Table 8. Revision history**

Date	Revision	Changes
05-Apr-2005	8	Modified value on <a href="#">Table 7.: Source drain diode</a>
26-Apr-2006	9	New template

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